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Docket No.: 02008/106002
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Seiji Ichiyoshi

Application No.: 10/813,594

Confirmation No.: 4387

Filed: March 30, 2004

Art Unit: 2138

For: TEST APPARATUS AND TEST METHOD

Examiner: J. C. Kerveros

INFORMATION DISCLOSURE STATEMENT (IDS)

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

22511
PATENT TRADEMARK OFFICE

Dear Sir:

Pursuant to 37 CFR 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO/SB/08. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is filed before the mailing date of a first Office Action after the filing of a Request for Continued Examination under 37 CFR 1.114 (37 CFR 1.97(b)(4)).

In accordance with 37 CFR 1.98(a)(2)(ii), Applicant has not submitted copies of U.S. patents and U.S. patent applications. Applicant submits herewith copies of foreign patents and non-patent literature in accordance with 37 CFR 1.98(a)(2).

A concise explanation of relevance of the items listed on form PTO/SB/08 is in the form of an English language copy of a Search Report from a foreign patent office, issued in a counterpart application, which refers to the relevant portions of the references.


In accordance with 37 CFR 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 CFR 1.56(a) exists. In accordance with 37 CFR 1.97(h), the filing of this Information Disclosure Statement shall not be construed to be an admission that any patent, publication or other information referred to therein is "prior art" for this invention unless specifically designated as such.

It is submitted that the Information Disclosure Statement is in compliance with 37 CFR 1.98 and the Examiner is respectfully requested to consider the listed references.

The Director is hereby authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith to our Deposit Account No. 50-0591, under Order No. 02008/106002.

Dated: May 4, 2007

Respectfully submitted,

By 

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Used in Lieu of PTO/SB/08A/B
(Based on PTO 04-07 version)

Substitute for form 1449/PTO			Complete if Known		
INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>			Application Number	10/813,594-Conf. #4387	
			Filing Date	March 30, 2004	
			First Named Inventor	Seiji Ichiyoshi	
			Art Unit	2138	
			Examiner Name	J. C. Kerveros	
Sheet	1	of	2	Attorney Docket Number	02008/106002

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	AA*	US-2003/0005375-A1	01-02-2003	Takasugi et al.	
	AB*	US-2001/016922 A1	08-23-2001	Takasugi et al.	
	AC*	US-5,425,036	06-13-1995	Liu et al.	
	AD*	US-5,991,907	11-23-1999	Stroud et al.	
	AE*	US-6,077,304	06-20-2000	Kasuya	
	AF*	US-6,108,806	08-22-2000	Abramovici et al.	
	AG*	US-6,202,182	03-13-2001	Abramovici et al.	
	AH*	US-2002/0038203-A1	03-28-2002	Tsuchiya	
	AI*	US-6,631,487	10-07-2003	Abramovici et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				
	BA	JP-2001-522049	11-13-2001	Credence Systems Corp.		
	BB	JP-2001-506367	05-15-2001	Simd Solutions Inc.		
	BC	JP-2000-267881	09-29-2000	Advantest Corp.		
	BD	JP-2002-141414	05-17-2002	Koninkl Philips Electronics NV		
	BE	JP-2001-320386	11-16-2001	Nippon Electric Co.		
	BF	JP-2000-163456	06-16-2000	Hitachi Ltd.		

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. * CITE NO.: Those application(s) which are marked with an single asterisk (*) next to the Cite No. are not supplied (under 37 CFR 1.98(a)(2)(iii)) because that application was filed after June 30, 2003 or is available in the IFW. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	CA	Explanation of Circumstances Relating To Accelerated Examination submitted in Japanese Application No. 2004-380598 dated March 1, 2007 and English translation thereof, 8 pages	
	CB	European Search Report issued in European Application No. EP 06 07 7162 dated February 23, 2007, 6 pages	
	CC	Xia J. Q. et al.: "Dynamic Test Emulation for EDA-Based Mixed-Signal Test Development Automation" Proceedings of The International Test Conference (ITC), Washington, Octo. 21-25, 1995, New York, IEEE, US, 761-770, XP000552879 ISBN: 0-7803-2992-9	
	CD	Castelnuovo A. et al.: "Emulation-Based Design Errors Identification" Defect and Fault Tolerance in VLSI Systems, 2002. DFT 2002. Proceedings. 17th IEEE International Symposium on 6-8 Nov. 2002, Piscataway, NJ, USA, IEEE, 6 November 2002 (2002-11-06), pages 365-371, XP010625026 ISBN: 0-7695-1831-1	
	CE	Japanese Office Action "Notification of Reasons for Rejection" issued in Japanese Application No. 2004-380598 mailed on April 3, 2007 and English translation thereof, 7 pages	
	CF	Dearborn, W. R., Perkins, E. G., Wong, J. J., Rolince, D., "The Virtual Test Program (V Test)", 1998 IEEE Autotestcon Proceedings, IEEE Systems Readiness Technology Conference, 1998	
Examiner Signature		Date Considered	

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Complete if Known	
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				Art Unit	2138
				Examiner Name	J. C. Kerveros
Sheet	2	of	2	Attorney Docket Number	02008/106002

		IEEE, U.S.A. IEEE, August 27, 1998, Catalog No. 98CH36179, pages 149-159	
	CG	U.S. Office Action issued in U.S. Application No. 10/404,002 mailed on April 9, 2007, 16 pages	

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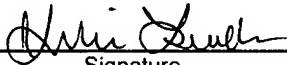
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Information Disclosure Statement (2 pages)
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